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Arithmetic core lphaAdditional info FPGA provenWishBone Compliant NoLicense LGPLDescriptionRTL Verilog code to perform Two Dimensional Fast Hartley Transform 2D FHT for 8x8 points Presented algorithm is FHT with decimation in frequency domain Main FeaturesHigh Clock SpeedLow Latency 97 clock cycles Low Slice CountSingle Clock Cycle per

Now let us try to understand the code This is multi line comment and this is single line comment Comments are same as in C language. Foreword by Frank Vahid gt HDL Hardware Description Language based design has established itself as the modern approach to design of digital systems with VHDL VHSIC Hardware Description Language and Verilog HDL being the two dominant HDLs.

In computer engineering a hardware description language HDL is a specialized computer language used to describe the structure and behavior of electronic circuits and most commonly digital logic circuits

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An arithmetic logic unit ALU is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers This is in contrast to a floating point unit FPU which operates on floating point numbers.

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